METHOD AND APPARATUS FOR DETERMINING CHARACTERISTICS OF MOS DEVICES

Field of the Invention

The present invention relates to semiconductors and, more particularly,

5   relates to metal oxide semiconductor (MOS) characterization.

Background of the Invention

The ability to measure the parameters of MOS devices is of great value, especially for technology development and accurate modeling of complementary MOS (CMOS) gate delays and leakage currents. The latter are important for circuit design

10   applications and chip power management. Two examples of MOS characteristics are the physical gate length (Lpoly) and gate oxide thickness (Tox) for MOS field effect transistors (MOSFETs), and these characteristics are extremely important for determining the performance of MOS circuits.

Direct current (DC) characteristics of a MOSFET provide a direct

15   technique for measuring threshold voltage, Vt, for the MOSFETs on a semiconductor. In CMOS technologies prior to generations having linewidths of about 0.18 μm, the effective length of the gate, Leff, was determined by extrapolation of the channel resistance of MOSFETs as a function of the designed gate length, Lmask. With the scaling of CMOS technologies, the scatter in the Leff measurement has become

20   significant, and Leff has now been replaced by the measurement of physical gate length, Lpoly. The Lpoly is generally estimated from the resistance of the film constituting the gate or from the gate oxide capacitance for a constant thickness of the gate oxide, Tox. As the physical gate oxide thickness is reduced below 1.5 nm (such as 0.13 μm linewidth technology generation and beyond), the DC tunneling current interferes with the

25   capacitance measurement.

Thus, what is needed are improved techniques for measuring characteristics of MOS devices.

Summary of the Invention

Methods and apparatus are presented for determining characteristics of

5   MOS devices.

In an aspect of the invention, a set of ring oscillators are provided. The set of ring oscillators is formed within a predetermined distance. Each ring oscillator includes a number of coupled stages. Each of the number of coupled stages for a first given ring oscillator includes an inverter having one or more first MOS devices having a

10   first gate length. Each of the number of stages for a second given ring oscillator includes an inverter substantially identical to the inverters in the coupled stages of the first ring oscillator plus one or more second MOS devices having a second designed gate length. Each of the number of stages for a third given ring oscillator includes an inverter substantially identical to the inverters in the coupled stages of the first ring oscillator plus

15   one or more third MOS devices having a third designed gate length. The second and third designed gate lengths are different and one of the second and third designed gate lengths is approximately equal to the first designed gate length. Performance is measured by using one or more of the given ring oscillators. The set of ring oscillators is used to determine one or more additional characteristics of MOS devices in the ring oscillators.

20   Beneficially, performance may be determined by causing a selected ring oscillator to oscillate so that a delay of a stage in the selected ring oscillator is under 30 picoseconds. Additionally, the predetermined distance in which the set of ring oscillators is formed may be 1,000 microns or less.

Advantages of the present invention include, but are not limited to, that

25   across-chip variations are minimized and that the characterization can occur using MOS devices similar or exactly equal to those used in the technology for high performance circuit applications and can occur at speeds similar to those attainable by the technology

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in high performance circuit applications. Moreover, many different characteristics of MOS devices may be obtained from the same set of ring oscillators.

For example, frequency of oscillation for the ring oscillators may be determined. The delay per stage for the ring oscillators may be determined by using the frequency of oscillation. The delay per stage is a measure of performance. The active and quiescent currents for the ring oscillators can be determined. The capacitance for the MOS devices making up a stage of each ring oscillator may be determined by using the active and quiescent currents and the delay.

In general, because the second and third designed gate lengths are different lengths, the capacitances associated with the second and third given ring oscillator stages should be different. These different capacitances may be used to determine a bias gate length, from which a physical gate length may be determined. The capacitances may also be used to determine the thickness of the oxide used in MOS gates. Additional characteristics may also be determined, such as effective gate resistance, gate tunneling current, channel leakage current per unit width, and active power.

In an illustrative embodiment, the set of ring oscillators are coupled together as a single test structure. Using the single test structure allows multiple MOS characteristics to be determined at one location and from the same set of test MOS devices so that design and layout variations between different test structures are not present. As described above, this also provides benefits of reduced across-chip variation in measurements and characteristics that may be determined under use conditions (e.g., delay of 30 picoseconds or less for a stage of a ring oscillator). The coupled ring oscillators can have outputs that pass through a single frequency divider, which is used to lower the frequency to an amount more easily read by a conventional frequency counting instrument. Additionally, outputs from the ring oscillators can be passed to a frequency counter, which can be integrated with the set of ring oscillators on a semiconductor. This, together with a clock, can generate an output indication of the frequency at which a ring oscillator is oscillating.

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Separate power supplies may be used for each of the ring oscillators and for control and output circuitry, which may be used to couple the ring oscillators together. A benefit, among others, of having separate power supplies is that the current drawn by an individual ring can be independently measured and the large current drawn by the

5 output driver does not affect the frequency of the ring oscillator. Additionally, each ring oscillator may be powered separately. Additional circuitry may be used to select only the powered ring oscillator for measurement purposes.

A more complete understanding of the present invention, as well as further features and advantages of the present invention, will be obtained by reference to the

10 following detailed description and drawings.

Brief Description of the Drawings

FIGS. 1A, 1B and 1C are examples of stages of ring oscillators, in accordance with preferred embodiments of the present invention;

FIGS. 2A, 2B and 2C are examples of capacitive loads for stages in ring

15 oscillators, in accordance with preferred embodiments of the present invention;

FIG. 3 is an example of a ring oscillator having a number of stages, in accordance with a preferred embodiment of the present invention;

FIG. 4 is an example of a circuit for determining characteristics of MOS devices, in accordance with preferred embodiments of the invention; and

20 FIG. 5 is a diagram used to determine Lbias.

Detailed Description of Preferred Embodiments

Conventional structures for determining metal-oxide-semiconductor (MOS) device characteristics have additional problems than those described previously. For example, the measurement of quantities such as the physical gate length, Lpoly, and

25 the thickness of the gate oxide, Tox, are determined by using separate test structures. Generally, the structures are created in the kerf area, which is an area surrounding active

chip areas, although the structures may also be placed in the active chip areas themselves. The measurements are repeated for each field effect transistor (FET) type offered by the technology. While Tox may be fairly uniform across a wafer, Lpoly may vary over a wide range across a chip. Lpoly variations may be local, depending on the surrounding patterns, or across a chip or wafer, depending on the gate lithographic and etch processes. Conventional methodology of using different test structures, physically separated from each other and embedded in a different optical Lpoly pattern, for each parameter measurement adds to the difficulty of making accurate correlation of these and other parameters with circuit function.

The present invention solves these problems by determining characteristics of MOS devices using a set of ring oscillators. Beneficially, a large number of characteristics may be determined from a single test structure having a set of ring oscillators. For example, in addition to performance (e.g., determined via gate delays of stages in ring oscillators), a single test structure may be used to determine physical gate length (Lpoly), gate oxide thickness (Tox), gate capacitance (C), effective gate resistance (Rsw), gate tunneling current (Ig), channel leakage current per unit width (Ic), active power (P), and additional characteristics. For ease of reference, the following disclosure is separated into two sections. The first section, entitled "Exemplary Apparatus," describes exemplary structures for determining MOS characteristics. The structures are stages and capacitive loads for ring oscillators, a ring oscillator, and a circuit containing a number of ring oscillators. The second section, entitled "Methods for Determining MOS Characteristics," describes exemplary steps using the structures described in the first section to determine characteristics of MOS devices.

Exemplary Apparatus

Turning now to FIG. 1A, an exemplary stage 100-1 used in a ring oscillator is shown. An example ring oscillator is described in more detail in reference to FIG. 3, and a number of ring oscillators are used to determine characteristics of MOS

devices, as described in more detail below. In FIG. 1A, stage 100-1 comprises a CMOS inverter 110-1. CMOS inverter 110-1 and other CMOS inverters described herein may be any set of devices used to invert a signal. Stage 110-1 will be referred to herein as a "reference stage." It is recommended that the CMOS inverter be the same CMOS inverter to be used for other MOS devices the technology will be used to create. The MOS gates (not shown) used in CMOS inverter 110-1 have a particular designed gate length, Lmask, of L1.

In FIG. 1B, stage 100-2 comprises a CMOS inverter 110-2 and a capacitive gate load 120-2. Exemplary capacitive gate loads are shown in FIGS. 2A through 2C. The capacitive gate load 120-2 is designed with a particular designed gate length, Lmask, of L2. In FIG. 1C, stage 100-3 comprises a CMOS inverter 110-3 and a capacitive gate load 120-3. The capacitive gate load 120-3 is generally designed with a particular designed gate length, Lmask, of L3. As described below, the different designed gate lengths, L2 and L3, may be used to determine load capacitance among other measurements.

In FIG. 2A, an exemplary capacitive gate load 200-1 is shown. Capacitive gate load 200-1 comprises an NMOS transistor 210-1 and a PMOS transistor 220-1. The NMOS transistor 210-1 has its source and drain coupled to ground, while the PMOS transistor 220-1 has its source and drain coupled to a power supply (e.g., Vdd). Capacitive gate load 200-1 is beneficial when it is desired to characterize the average of NMOS and PMOS devices with one capacitive gate load.

Nonetheless, it can be beneficial to split the NMOS and PMOS devices into separate capacitive loads, as this can allow better determination of capacitance for each of the NMOS or PMOS devices. This splitting is shown in FIGS. 2B and 2C. In FIG. 2B, an exemplary capacitive gate load 200-2 is shown. Capacitive gate load 200-2 comprises two NMOS transistors 210-2 and 220-2. The NMOS transistors 210-1 and 220-2 have their sources and drains coupled to ground. In FIG. 2C, an exemplary capacitive gate load 200-3 is shown. Capacitive gate load 200-3 comprises two PMOS

transistors 210-3 and 220-3. The PMOS transistors 210-3 and 220-3 have their sources and drains coupled to a power supply (e.g., Vdd).

Although two devices per capacitive gate load 200 are shown, each capacitive gate load can comprise more or less devices. For instance, a capacitive gate load 200 could comprise a single device or four devices.

Referring now to FIG. 3, a ring oscillator 300 is shown. Ring oscillator 300 comprises, in this example, 100 stages 310-1 through 310-100. The use of 100 stages is merely exemplary, and ring oscillator 300 may comprise many different numbers of stages. Each stage 310 is generally one of the stages 100-1, 100-2 or 100-3 of FIGS. 1A through 1B, and stages usually are not mixed in one ring oscillator. In other words, each state 310 will be one and only one of the stages 100-1, 100-2 or 100-3. In FIG. 3, a stage such as stage 100-2 of FIG. 2A is shown. Each stage 310 comprises a CMOS inverter 320 and a capacitive gate load 330. The ring oscillator 300 also comprises a NAND gate 340 and an output 350. The NAND gate 340 is used to enable or disable oscillations. The output 350 may be passed to a frequency divider and frequency counter, as shown in FIG. 4 or directly to an on-chip frequency counter (not shown). It should be noted that there are multiple possible locations for the output 350, and the location shown is merely exemplary.

Reference 350 illustrates a delay 360 for stage 310-99. A delay 360 occurs from the middle of the rise to the middle of the descent for a stage, such as stage 310-99. The delay 360 is a measure of performance for a stage of the ring oscillator 300. Delay 300 is preferably less than 30 picoseconds or whatever a suitable delay is for the technology being used to create the stages.

Multiple ring oscillators 300 may be uncoupled and data extracted from each of the ring oscillators 300. However, it is beneficial to form one circuit that couples multiple ring oscillators 300 and from which many MOS characteristics may be determined, as this limits across-chip effects and provides interface simplicity. One example of a single circuit having multiple ring oscillators is shown in FIG. 4.

Turning now to FIG. 4, a circuit 400 for determining characteristics of MOS devices is shown. Circuit 400 may be used to determine a number of characteristics of MOS devices. Exemplary characteristics are described below. Circuit 400 is generally formed in a kerf area of a semiconductor but may be placed in any suitable location.

5   Circuit 400 is shown connected, in this example, to an external frequency counter. Circuit 400 comprises five ring oscillators 410-1 through 410-5 that are formed within a distance 490. Distance 490 is preferably less than 1,000 microns to reduce across-chip effects from affecting characterization. Each ring oscillator 410 has its own power supply 404 and current sensor 405. Circuit 400 further comprises a number of CMOS inverters

10   420-1 through 420-15, NAND gates 430-1 through 430-4, and frequency divider 440.

       The ring oscillators 410 are enabled by using the S input 403. The measurement circuitry 470 uses a separate power supply 404-6 in order to minimize effects caused by using the same power supply for the measuring as for running the ring oscillators 410 and to allow independent current measurements on individual rings.

15   Additionally, this allows each ring oscillator 410 to be separately powered on via one of the power supplies 404-1 through 404-5. Ring oscillators 410 are selected via the measurement circuitry 470. The portion of the measurement circuitry 470 beneath the ring oscillators 410 (i.e., NAND gates 430-1 through 430-4 and inverters 420-1 through 420-12) performs an OR function on the ring outputs such that the output of the single

20   ring that is powered and selected is directed through the frequency divider 440 and output driver 445.

       In this example, the frequency counter 450 is not part of the circuit 400. Instead, it is a separate conventional instrument used to measure frequency. However, the frequency counter 450 may be integrated into the chip design as part of the counter 450,

25   generally by placing the frequency counter 450 between the frequency divider 440 and output driver 445, or by eliminating the frequency divider 440 altogether and using a clock input together with a counter to measure the ring oscillator frequency. The frequency counter 450 has an output 460, which allows a frequency to be determined.

The output 460 can be a set of lines indicating a binary value convertible to frequency, for instance.

The S input 403 and voltage supplies 404 can be enabled in a number of ways. For instance, the S input 403 and voltage supplies 404 can be routed to pads, and voltage can be placed on the pad through various devices. A ring oscillator is enabled by applying voltage to the input power supply 404, generally at a pad (not shown), followed by applying a voltage to the S input 403, also generally at a pad (not shown).

In the example of FIG. 4, ring oscillator 410-1 corresponds to a ring oscillator having stages 110-1 of FIG. 1A. Ring oscillator 410-2 corresponds to a ring oscillator having stages 100-2 of FIG. 1B, where the stages 100-2 include the NMOS capacitive gate load 200-2 shown in FIG. 2B, with an Lmask of L2. The inverters (not shown) used in stages 110-2 of ring oscillator 410-2 are substantially identical to the inverters used in stages 110-1 of ring oscillators 410-1. "Substantially identical" generally means that the designs for the inverters in the stages 110-1 and 110-2 are the same, although slight differences in the physical inverters 110-1 and 110-2 might exist. Ring oscillator 410-3 corresponds to a ring oscillator having stages 100-3 of FIG. 1C, where the stages 100-3 include the NMOS capacitive gate load 200-2 shown in FIG. 2B, with an Lmask of L3. Ring oscillator 410-4 corresponds to a ring oscillator having stages 100-2 of FIG. 1B, where the stages 100-2 include the PMOS capacitive gate load 200-3 shown in FIG. 2C, with an Lmask of, for instance, L2. Ring oscillator 410-5 corresponds to a ring oscillator having stages 100-3 of FIG. 1C, where the stages 100-3 include the PMOS capacitive gate load 200-3 shown in FIG. 2C, with an Lmask of, for instance, L3. It should be noted that it is recommended that each inverter in the stages of the ring oscillators 410 be the same inverter. That is, it is recommended that each inverter have the same designed gate length for the NMOS and PMOS devices therein.

Thus, ring oscillator 410-1 includes reference stages, ring oscillators 410-2 and 410-3 include NMOS stages having two different Lmasks, and ring oscillators 410-4

and 410-5 include PMOS stages having two different Lmasks. This configurations allows accurate characteristic an individual measurements for both NMOS and PMOS devices.

As another example, three ring oscillators 410-1 could be used. In this second example (which is used as one of the bases for the methods given below), ring oscillator 410-1 corresponds to a ring oscillator having stages 110-1 of FIG. 1A. Ring oscillator 410-2 corresponds to a ring oscillator having stages 100-2 of FIG. 1B, where the stages 100-2 include the NMOS/PMOS capacitive gate load 200-1 shown in FIG. 2A, with an Lmask of L2. Ring oscillator 410-3 corresponds to a ring oscillator having stages 100-3 of FIG. 1C, where the stages 100-3 include the NMOS/PMOS capacitive gate load 200-1 shown in FIG. 2A, with an Lmask of L3.

Thus, in this second example, ring oscillator 410-1 includes reference stages, while ring oscillators 410-2 and 410-3 include NMOS/PMOS capacitive loads having different Lmasks.

Methods for Determining MOS Characteristics

Now that the apparatus used to determine characteristics of MOS devices have been described, methods for determining MOS characteristics by using the apparatus is described. The following method uses the second example above, which uses three ring oscillators. The first ring oscillator has stages of inverters. The second ring oscillator has stages of inverters along with NMOS/PMOS load devices, as shown in FIG. 2B, with a relatively small Lmask. The third ring oscillator has stages of inverters along with NMOS/PMOS load devices, as shown in FIG. 2B, with a relatively large Lmask.

Lpoly and Tox are derived by using a difference technique, which eliminates the influence of unknown parasitic resistances and capacitances and allows the influence of each component (i.e., Lpoly and Tox) to be separated from the measurement.

The measurements made include the following: ring oscillator frequency, f; current drawn when the ring is switching, Ia; and current drawn when the ring is

quiescent, Io. The delay per stage, D, is calculated from the measured ring oscillator frequency as follows:

$$D = 1/(2 * n * f), \tag{1}$$

where n is the number of stages in the ring. The load capacitance per stage is given by the
5 following:

$$C = 2 * (Ia - Io) * D / Vdd, \tag{2}$$

where Vdd is the power supply voltage. The delay and capacitance per stage for the three ring oscillators are denoted by D1, D2, D3 and C1, C2 and C3, respectively. The capacitance is usually measured at 0.8X the nominal supply voltage for the technology
10 and the short circuit power is negligible.

a) Determination of Lpoly

The load capacitance CG1 (i.e., C2 - C1) and CG2 (i.e., C3 - C1) are plotted against Lmask in FIG. 5. As previously described, the Lmask is the Lpoly design dimension. It should be noted that the Lmask is the "stepped down" dimension that
15 should appear on the surface of a semiconductor. The intercept on the x-axis gives the bias length, Lbias, where Lpoly = Lmask - Lbias. More than three ring oscillators may be used for better accuracy as is the case in FIG. 5, where four ring oscillators have been used. Lbias is generally calibrated against measurements made on physical cross-sections using a scanning electron microscope as practiced currently with the capacitance or
20 resistance tests structures. This introduces a one-time, per-technology, fixed adjustment to Lbias that takes into account fringe field effects. The techniques described herein are then used on a regular bases, along with this fixed adjustment, to monitor and track Lpoly and other characteristics.

b) Determination of Tox

The effective gate oxide thickness, Tox, may be determined as

$$Tox = k \, (L3mask - L2mask) * W / (C3 - C2), \qquad (3)$$

where k is the dielectric constant, and W is the width of the gate. This result is totally
independent of Lbias.

c) Simultaneous Determination of other MOSFET Parameters

There are several other MOSFET parameters that can be directly
determined from the same product representative ring oscillators, such as used in circuit
400 of FIG. 4, used to determine Lpoly and Tox. While these other parameters could be
determined from other structures, it is extremely valuable to have this information all
coming from the same structures used to determine Lpoly and Tox, as this then provides a
self consistent set of data free from the effects of across-chip linewidth variation (ACLV)
and other variations coming from, for example, different local environments.

The gate delay, which is a direct measure of performance, is already
known from Equation (1).

The gate delay is related to the effective gate resistance, Rsw, during
switching. The effective gate resistance is the inverse of the gate drive strength and
related to Vt as follows:

$$Rsw = (D2 - D1) / (C2 - C1). \qquad (4)$$

The gate tunneling current, Ig, per unit area is given by the following:

$$Ig = (Io3 - Io1) / \{2 \, n * (W * (L3mask - L2mask))\} \qquad (5)$$

As with the equation for Tox, the evaluation of Ig in no way involves knowledge of Lbias. The channel leakage current per unit width, Ic, averaged over NMOS and PMOS is given by

$$Ic = (Io1 / n) - Ig * Lpoly * (Wn + Wp) / 2 \qquad (6)$$

The active power P is given by

$$P = (Ia - Io) * Vdd = 0.5 * C * Vdd^2 / D, \qquad (7)$$

where C is the effective total capacitance.

The short circuit power at a supply voltage Vdd1 is as follows:

$$Psc = P(Vdd1) - 0.5 * C * Vdd1^2 / D \qquad (8)$$

where $Vdd < Vdd1$ and C is determined from Equation (7).

d) Other MOSFET and Wire Parameters

The difference technique may be extended to measurement of wire resistances and capacitances, delay and leakage currents as a function of stack height in stacked gates (NANDs and NORs) and Rsw of different gate types. The contributions of NMOS and PMOS may be separated by making the gate delay dominated by either the NMOS or PMOS. It may also be used to estimate and calibrate parasitic resistances and capacitances by implementing different layout schemes.

It is to be understood that the embodiments and variations shown and described herein are merely illustrative of the principles of this invention and that various modifications may be implemented by those skilled in the art without departing from the

scope and spirit of the invention. For instance, each of the ring oscillators in circuit 400 of FIG. 4 may be individually created and data extracted separately from each. Generally, each ring oscillator would then have a frequency divider and output driver associated with it. Each ring oscillator may also have a frequency counter associated with it. Additionally, there may be multiple different ring oscillators used, a set of the ring oscillators having different designed gate lengths. This allows, as shown in FIG. 5, a better determination of Lbias.